**EE466 Course Project**

**Due Date: Dec.7,2023**

1. **Design of implicit pulse semidynamic Flip flop(ip-DCO)**

How it works

The cascaded inverter C1 delays the clock signal. If the clock is 0, T1 is turned on and T2 and T6 is turned off. However, T4 is turned on.

When D is 0, T3 is turned off. when the clk signal is 0, n1 is ON, and T2 is off and T4 is On, this charges n2 to VDD. T7 is off and T6 is off but T5 is ON. When the clock switched from 0 to 1, T6 is turned on and n3 is discharged so that Qbar becomes 1.

when D=1, T3 is turned on. when n1 is 0, T2 is on, T4 is off and T7 is on T6 is on, this charges n3 to VDD, and n3 becomes logic 1 and Qbar becomes 0. When clock signal goes low, and D=1, T1 is turned on, T2 is off and T3 and T4 are off.

2. Delay 2.07

Power comsumption: ivdd \* current = -6.7688\*10^-6

Area:143550

The waveforms of signals are included below:

A diagram of a circuit

Description automatically generated

A screen shot of a computer

Description automatically generated

1. **Design of Hybrid Latch Flip flop -Paper2 Fig(1)**

**A diagram of a circuit

Description automatically generated**

How it works

When the clock is 0, P1 is on and N3 is ON, N1 and N4 are off and X is precharged to VDD. When the clock is 1, N1 and N4 turns on, this charges the inverter at node Q. If D=0, node Q=0 and QB=1. However when node CKDB become 0, node X becomes decoupled from D and begins to charge to VDD by P3.

The waveforms of signals from the clock, nD, nQ and nQbar is included below

A screen shot of a computer

Description automatically generated

Delay 2.01

Power comsumption: ivdd \* current = -8.0969\*10^-5(from 1ns to 3ns)

Area:5470650

1. **Design of Semidynamic edge triggered flip flop Paper 3 Fig(3)**

**A diagram of a circuit

Description automatically generated**

How it works

The cascaded inverter delays and inverts the clock signal which is NANDed with X. When the clock is 0, N3 is off and S is almost always on due to the NAND gate. At this point 0 from the NAND gate and 1 from P1 keep node S which keeps N1 on. P1 is on and node X is charged to VDD. P2 is off and inv5-6 keeps the previous charge of Q. When clk goes high, node S goes low after some delay. If D=0, N4 and N5 turns on and discharges Q. Then QB goes high.

When D is high when the clock goes high, transistors N1, N2,N3 turns on and discharges X. This turns P2 on and Q, then QB becomes low.

A screen shot of a graph

Description automatically generated

Delay 144ps

Power comsumption: ivdd \* current = -2.0116\*10^-4(from 3ns to 7ns)

Area: 43465050nm^2

1. **Design of Time-borrowing static master-slave (tb-SMS) Paper1 Fig(3)**

A diagram of a circuit

Description automatically generated

How it works

When the clock is low, and D is 0, P1 is turned on, P2 is turned off, Qbar is 0, making Q go to high. When D is high, N1 is turned on, N2 is off, which makes Q high. However when the clock is high, P2 is high and Q is low.

Delay 144ps

Power comsumption: ivdd \* current = -4.7706\*10^-6(from 3ns to 7ns)

Area:148050nm^2

A screen shot of a graph

Description automatically generated

1. **Design of Explicit-pulsed flip-flop EP-sFF Paper1 Fig(5)**

**A diagram of a circuit

Description automatically generated**

How it works

The output of the cascaded inverter is NAND with the clock signal. When the clock high, node n1 is on. When D = 1, R1 charges to VDD and Qbar is low. After some delay of inverter chain, N1 is turned off, if D =0, Qbar becomes high.

A screenshot of a computer

Description automatically generated

Delay 23ps

Power comsumption: ivdd \* current = -1.0005\*10^-6watts(from 3ns to 7ns)

Area:928,350nm^2

1. **Design of Explicit-pulsed flip-flop EP-sFF Paper1 Fig(9)A diagram of a block diagram

   Description automatically generated**

A screen shot of a computer

Description automatically generated

Delay 23ps

Power comsumption: ivdd \* current = -1.059\*10^-5watts(from 3ns to 7ns)

Area:6,418,350nm^2

How it works

The output of the cascaded inverter is NAND with the clock signal. When the clock high, node n1 is on. When D = 1, R1 charges to VDD and Qbar is low. After some delay of inverter chain, N1 is turned off, if D =0, Qbar becomes high.